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EXAMINER	
LEUNG, CHRISTINA Y	
ART UNIT	PAPER NUMBER
2633	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,608	LIGHT, GRETA	
	Examiner	Art Unit	
	Christina Y. Leung	2633	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 14 is objected to because of the following informalities:

Claim 14 currently recites "wherein the connector configured to interface" (sic) in lines 1 and 2 of the claim. Examiner respectfully suggests that Applicant amend the phrase to "wherein the connector *is* configured to interface" for grammatical reasons.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Benzoni et al. (US 5,337,398 A).

Regarding claim 1, Benzoni et al. disclose an optical device (Figures 1-14, particularly Figures 1, 6, and 11-13) comprising:

a housing (including outer package 60 shown in Figure 12; column 7, lines 16-26);

at least one optical subassembly (including light emitting diode LED 26 and photodiode 28 shown in Figures 6 and 12 and ferrule receptacles 50 and 52 shown in Figure 12; column 4, lines 44-47; column 6, lines 37-39) substantially disposed within the housing and defining a longitudinal axis (i.e., the axis shown in Figure 12 as a dashed line along the ferrule receptacles,

vertical with respect to the page; this axis corresponds to the axis pointing out of the page in the view of Figure 6);

a substrate 12 substantially disposed within the housing and residing in a plane that is substantially perpendicular to the longitudinal axis defined by the at least one optical subassembly, the substrate including electronic circuitry (such as transmitter circuit 18 and receiver circuit 20; column 4, lines 2-47); and

a connector (including leads 16) disposed on one end of the substrate and mounted on a surface of the substrate within the plane that is substantially perpendicular to the longitudinal axis (Figures 11-13 show how the substrate 12 and connector leads 16 define a plane that is perpendicular to the axis of light transmitted and received through the ferrule receptacles 50 and 52).

Regarding claim 2, Benzoni et al. disclose that the at least one optical subassembly comprises at least one of: a transmit optical subassembly (including LED 26) and a receive optical subassembly (including photodiode 28; column 4, lines 44-47).

Regarding claim 3, Benzoni et al. disclose that the connector 16 is in electrical communication with at least some of the electronic circuitry of the substrate (Figure 3, for example, clearly shows the electrical connections between connector leads 16, the transmitter and receiver circuits 18 and 20, LED 26, and photodiode 28).

Regarding claim 5, Benzoni et al. disclose that the at least one optical subassembly is mechanically and electrically connected to the substrate (Figure 3 shows the electrical connection of the LED 26 and photodiode 28 of the subassemblies to the substrate 12; Figure 12

shows the physical connection of the extended ferrule receptacles 50 and 52 of the subassemblies to the substrate 12).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 4, 6-12, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Benzoni et al. in view of qLogic ("SANblade: 2-Gbps Fibre Channel to PCI Express Host Bus Adapter," dated 09/03 by qLogic Corporation).

Regarding claim 4, Benzoni et al. disclose a system as discussed above with regard to claims 1 and 3 above, including leads 16 which inherently enable the disclosed transceiver elements to be connected to another device, but they do not specifically disclose connecting the transceiver to a host bus adapter. However, qLogic teaches a host bus adapter including an optical transceiver such as already disclosed by Benzoni et al. Regarding claim 4, it would have been obvious to a person of ordinary skill in the art to use the host bus adapter taught by qLogic with the transceiver disclosed by Benzoni et al. in order to enable the optical transceiver to be readily installed in a host using standardized physical slots.

Regarding claim 6, Benzoni et al. disclose an optoelectronic interface device, comprising:

an optical transceiver (Figures 1, 6, and 11-13) configured to mechanically and electrically interface with another device (via connector leads 16) and comprising:

a housing (including outer package 60 shown in Figure 12; column 7, lines 16-26);

a transmit optical subassembly (light emitting diode LED 26 and associated ferrule receptacle 50 shown in Figure 12) and a receive optical subassembly (photodiode 28 and associated ferrule receptacle 52) substantially disposed within the housing, each of which defines a corresponding longitudinal axis (i.e., the axis shown in Figure 12 as a dashed line along the ferrule receptacles, vertical with respect to the page; this axis corresponds to the axis pointing out of the page in the view of Figure 6; column 4, lines 44-47; column 6, lines 37-39); and

a transceiver substrate 12 substantially disposed within the housing and residing in a plane that is substantially perpendicular to the longitudinal axes respectively defined by the transmit optical subassembly and the receive optical subassembly, the transceiver substrate including electronic circuitry (including transmitter circuit 18 and receiver circuit 20; column 4, lines 2-47); and

a connector (leads 16) located on an end of the transceiver substrates the connector mounted on a surface of the transceiver substrate in the plane that is substantially perpendicular to the longitudinal axes (Figures 11-13 show how the substrate 12 and connector leads 16 define a plane that is perpendicular to the axis of light transmitted and received through the ferrule receptacles 50 and 52).

Benzoni et al. disclose leads 16 which inherently enable the disclosed transceiver elements to be connected to another device, but they do not specifically disclose connecting the transceiver to a host bus adapter.

However, qLogic teaches a host bus adapter, including an optical transceiver such as already disclosed by Benzoni et al. qLogic further teaches that the host bus adapter has a printed

circuit board and at least one connector (i.e., an array of pins on the board) for electrically interfacing with a host device.

Further regarding claims 7 and 8 in particular, qLogic further teaches a host bus adapter that is configured to be substantially received within a standard PCI card slot of the host device (see third item under "Features" on page 1)

Regarding claims 9, 10, and 11, qLogic further teaches a host bus adapter comprising a printed circuit board for a peripheral component interconnect (PCI) card, further comprising a face plate defining cutouts and being attached, at least indirectly, to at least one of a optical transceiver and, the host bus adapter (see Figure on page 1), and wherein the faceplate includes at least one status indicator (see eighth item under "Features" on page 1).

Regarding claims 6-11, it would have been obvious to a person of ordinary skill in the art to use the host bus adapter taught by qLogic with the transceiver disclosed by Benzoni et al. in order to enable the optical transceiver to be readily installed in a host device using standardized physical slots and also in order to provide status indicators to monitor the operation of the transceiver.

Regarding claim 12, Benzoni et al. disclose an optical transceiver (Figures 1, 6, and 11-13) comprising:

a housing (including outer package 60 shown in Figure 12; column 7, lines 16-26);

a transmit optical subassembly substantially disposed within the housing and defining a longitudinal axis (light emitting diode LED 26 and associated ferrule receptacle 50, defining an axis shown as a dashed line in Figure 12);

a receive optical subassembly substantially disposed within the housing and defining a longitudinal axis (photodiode 28 and associated ferrule receptacle 52, defining an axis shown ias a dashed line in Figure 12);

a transceiver substrate 12 substantially disposed within the housing and residing in a plane that is substantially perpendicular to the longitudinal axes respectively defined by the transmit optical subassembly and the receive optical subassembly (Figures 11-13 show how the substrate 12 defines a plane that is perpendicular to the axis of light transmitted and received through the ferrule receptacles 50 and 52);

the transceiver substrate including electronic circuitry (including transmitter circuit 18 and receiver circuit 20; column 4, lines 2-47), and the transceiver substrate being physically and electrically connected to the transmit optical subassembly and the receive optical subassembly (Figure 3 shows electrical connections between substrate 12 and LED 26/photodiode 28 of the subassemblies; Figure 12 shows the physical connections between substrate 12 and the ferrule receptacles of the subassemblies); and

a connector (leads 16) connected to the transceiver substrate, the connector mounted at a surface of the transceiver substrate in the plane, wherein the connector electrically and mechanically connects the transceiver substrate to another device.

Benzoni et al. disclose leads 16 which inherently enable the disclosed transceiver elements to be connected to another device, but they do not specifically disclose connecting the transceiver to a host bus adapter.

However, again, qLogic teaches a host bus adapter that is a PCI card including an optical transceiver such as already disclosed by Benzoni et al. Regarding claim 14 in particular, qLgoic

teaches connecting the host bus adapter to an optical transceiver such that the transceiver is at an edge of the adapter (see Figure on page 1). Regarding claim 15 in particular, qLogic teaches that the host bus adapter is a PCI card.

Regarding claims 12, 14, and 15, it would have been obvious to a person of ordinary skill in the art to use the host bus adapter/PCI card taught by qLogic with the transceiver disclosed by Benzoni et al. in order to enable the optical transceiver to be readily installed in a host using standardized physical slots. Further regarding claim 14 in particular, it also would have been obvious to a person of ordinary skill in the art to connect the transceiver to an edge of the host bus adapter as suggested by qLogic so that the ferrule receptacles of the transceiver as disclosed by Benzoni et al. are located on the outside of the overall system and thereby more conveniently allow optical fibers to be attached to the system.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Benzoni et al. in view of qLogic as applied to claim 12 above, and further in view of Dwarkin et al. (US 6,454,470 B1).

Regarding claim 13, Benzoni et al. in view of qLogic describe an optical transceiver as discussed above with regard to claim 12, but they do not specifically disclose data rates at least 10 Gbps. However, Dwarkin et al. teach optical transceivers that are used in connection with 10 Gbps data rates (column 1, lines 43-44). It would have been obvious to a person of ordinary skill in the art to use optical transceiver elements suitable for 10 Gbps data rates as taught by Dwarkin et al. in the system described by Benzoni et al. in view of qLogic in order to transmit data more efficiently.

7. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Benzoni et al. in view of qLogic as applied to claim 12 above, and further in view of Giboney et al. (US 6,318,909 B1).

Regarding claim 16, Benzoni et al. in view of qLogic describe an optical transceiver as discussed above with regard to claim 12 including a transceiver substrate defining front and rear sides and having electronic circuitry. They do not specifically disclose disposing the circuitry on both the front and rear sides of the substrate, but Giboney et al. teach a system related to the one disclosed by Benzoni et al., including an optical transceiver and a transceiver substrate 25 (Figures 1A and 1E). Giboney et al. further teach placing circuitry on both sides of the transceiver substrate (column 9, lines 46-54). It would have been obvious to a person of ordinary skill in the art to place circuitry on both sides of the transceiver substrate as taught by Giboney et al. in the system described by Benzoni et al. in view of qLogic in order to more efficiently use the area of the substrate and thereby advantageously allow the circuitry to fit in a smaller overall area.

Response to Arguments

8. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christina Y. Leung whose telephone number is 571-272-3023. The examiner can normally be reached on Monday to Friday, 6:30 to 3:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Chan can be reached on 571-272-3022. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2600.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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